IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Application Of:			
	Snyder	Examiner:	Phan, T.
Serial No.:	09/975,104	Art Unit:	2128
Filing Date:	10/10/01	Conf. No.:	8786
For:	CAPTURING TEST/EMULATION AND ENABLING REAL-TIME DEBUGGING USING AN FPGA FOR IN-CIRCUIT EMULATION		

RESPONSE TO FINAL OFFICE ACTION ACCOMPANYING RCE

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

In response to the Office Action mailed February 15, 2006 for the above captioned patent application, and per the Request for Continued Examination filed herewith, Applicant respectfully requests entry of the following amendments and consideration of the following remarks.